Model-based scanner tuning in a manufacturing environment

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ABSTRACT

Given the decrease in k1 factor for 65nm-node lithography technology and beyond, it is increasingly important to understand and control the variables which impact scanner imaging behavior in the lithography process. In this work, we explore using model simulations to characterize and predict imaging effects of these variables, and then based on such information to fine-tune the scanner settings to obtain printing results optimally matched to a reference scanner. The scanner modeling makes use of detailed scanner characteristics as well as wafer CD measurements for accurate model construction. To identify critically mismatched patterns on a production layout, we employ the fast full-chip simulation capability provided by Brion's Tachyon servers. Tachyon simulations are also used to predict wafer impacts of changes in tunable scanner parameters. A set of optimized scanner variable offsets, called a "scanner tuning recipe", is generated to minimize overall imaging mismatch between two scanners. As a proof-of-concept, we have carried out scanner tuning procedures on selected ASML scanners. The results show improvements more than 20% on CD offset RMS values for 2D line-end patterns, production layout patterns, and the mismatched patterns identified with the full-chip simulation. Improvements on wafer-acceptance-test results and production yield on the to-be-tuned scanner are also observed.

Keywords: scanner tuning, model-based, scanner matching, manufacturing environment, low k1 imaging

1. INTRODUCTION

In cutting-edge low-k1 lithographic processes, precise control and active tuning of the lithographic parameters have become more important than ever for the optimization of manufacture yield and production quality. A typical use case is the tuning of the optical parameters on one scanner to optimize its imaging performance for a particular production layout so that it's matched to that of a reference scanner [12]. Such optimizations rely on the accurate understanding of how the changes of scanner parameters impact imaging of the layout patterns of interest, called "matching targets". In addition to the generic patterns independent of any production layout, the matching targets may also include the patterns identified on a production layout to be more likely to fail on the to-be-tuned scanner, or "weak spots". The conventional practice of using purely experimental methods to perform the optimization is becoming unfeasible due to the large number of distinct weak spots that may exist on a full-chip production layout, and the increasing number of lithographic parameters available in the tuning. We have adopted a method of model-based scanner tuning, which is analogous to model-based optical proximity correction (OPC), in that adequately characterized lithography models, instead of extensive and iterative wafer exposure experiments, are used to drive the optimization.

Compared to OPC, scanner tuning has different and often more stringent requirements on the prediction accuracy of the model. Therefore, the model calibration approach needs to be customized to meet the requirements, and more scanner characteristics data are needed. Once the models are calibrated, simulations can be performed to obtain a) the effect of scanner parameter changes on arbitrary layout patterns, b) the effect that the differences between the two scanners can produce on arbitrary layout patterns, and c) the "matching weak spots" on a production layout that are more likely than others to fail when manufactured with the to-be-tuned scanner. The last result, in particular, requires fast full-chip simulation capacities for the procedure to be practical in a manufacturing environment. These simulation results are then used to guide the scanner tuning, and a modified set of scanner parameters is generated, optimized for manufacturing the product in question. The procedure described above for scanner tuning is referred to as "LithoTuner" in this work, after the Brion product LithoTuner™ PatternMatcher FullChip based on this procedure.

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In this work, we show the application of the above procedure on a real manufacturing process for 65nm-node ("N65") poly using a real production layout. Compared to conventional approaches that only optimize for a limited number of pre-established performance-critical patterns, we have demonstrated substantial improvements on matching weak spots in the design (complex 2-dimensional patterns and gate features), while retaining a comparable CD uniformity (CDU) on the critical line/space patterns. Wafer-acceptance-tests and yield analysis have shown that the tuning can also improve the wafer-acceptance-test results, and increase production yield of the product on the to-be-tuned scanner to the same level as on the reference scanner.

2. METHODOLOGY

The lithographic models used in OPC are calibrated by exposing photomasks containing test patterns, taking wafer measurements for the test patterns, and adjusting certain empirical model parameters so that the model predictions can be best fitted to the experimental wafer data. The OPC models are used for full-chip simulations, so they need to have good prediction accuracy on arbitrary layout patterns. This prediction accuracy, however, is only required under a fixed lithographic condition plus possible focus and exposure dose variations. For scanner tuning models, there is the additional requirement that the prediction accuracy must be maintained under any lithographic condition that may constitute a valid tuning result. On the other hand, in the context of scanner matching, it is often sufficient to achieve the "differential prediction accuracy", which is the accuracy in predicting the changes on wafer as induced by differences in scanner settings, instead of the absolute accuracy in prediction of the wafer pattern contours.

To address the specific requirements in scanner tuning, we have developed an "extended focus-exposure-matrix (FEM)", or "super FEM" approach to calibrate the lithographic models, as an extension to the focus-exposure-matrix modeling approach employed in calibration of Tachyon OPC models. In FEM modeling for OPC models, wafer measurements taken under different focus and exposure dose values are used to jointly calibrate a single set of empirical model parameters, such that the model, when supplied with the appropriate focus and dose values, remains accurate throughout the focus/exposure process window[3]. Similarly, in the "super FEM" approach, wafer measurements are taken under both the "nominal" optical condition and "perturbed" conditions, which differ from the nominal condition by small perturbations of scanner parameters (NA, outer and inner sigma, focus, dose, EFESE, ellipticity), and together they are used in the model calibration. Detailed scanner characteristics data, such as illumination source measurements, projection pupil aberration measurements, laser bandwidth/spectrum, stage vibration, etc., are also necessary for the calibration, as better knowledge of the actual scanner conditions corresponding to the wafer measurements allows a better separation between the imaging effects of the scanner conditions and those of the resist process, and thus the scanner imaging behavior can be predicted with higher accuracy.

One critical aspect in lithographic model calibration is the selection of test patterns that are used as experimental agents to capture the characteristics of the process and drive the model calibration. Insufficient test pattern coverage impairs model prediction accuracy, whereas an excessive amount of test patterns comes with the heavy burden of prolonged wafer metrology time. For scanner matching purposes, the constraint in wafer metrology time is particularly tight, since wafer data need to be taken under multiple optical conditions. We have developed dedicated algorithms to address the problem of selecting from a general-purpose test reticle the most effective test patterns for pinpointing the model parameters for a given nominal process condition. The typical number of test patterns to be measured for each optical condition can be reduced to the order of 100, as opposed to the >~1000 test patterns regularly used in OPC model calibration.

Based on Tachyon models adequately calibrated using the approach above, we can predict the effects that the changes to the tunable scanner parameters, or "scanner knobs", have on the imaging of arbitrary mask patterns, also known as the patterns' "sensitivity" to scanner knobs.

In addition to accurate predictions of the sensitivities to the scanner knobs, the differences between the reference scanner and the to-be-tuned scanner in terms of imaging behavior also need to be predicted accurately by the model (the "differential accuracy" requirement). Good differential accuracy enables the scanner tuning to take into consideration the patterns for which wafer metrology data are not available, e.g., matching targets identified in full-chip simulation. To achieve this goal, wafer measurement data are taken from both scanners for selected test patterns, and the models not only utilize the two sets of comprehensive scanner characteristics data for both scanners, but also go through parameter optimizations based on the wafer data, so that the model-predicted differences can best match the measured wafer differences between the two scanners. The procedure above is referred to as "differential calibration".

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With both sensitivity accuracy and differential accuracy achieved, the optimization of scanner tuning recipes can be performed for the to-be-tuned scanner, to match its imaging behavior to that of the reference scanner.

3. RESULTS

3.1 Test conditions

For proof-of-concept of the LithoTuner methodology, two ASML scanners are chosen to carry out the experiments. The nominal optical conditions are optimized for the production of the poly layer for N65 technology node.

3.2 Test pattern selection and model calibration

For the optical condition being used, we have selected from ASML's Proxi-45 reticle (a generic test reticle) 500 patterns for nominal condition wafer exposure and 100 patterns for perturbed condition wafer exposures. We have also designed five different perturbed optical conditions, optimized for the calibration procedure. Altogether 500*1 + 100*5 = 1000 distinct wafer data points are taken for the calibration of the scanner model. Detailed scanner parameters are measured and fed into Brion's Tachyon model calibration engine. Shown in Figure 1 is an example of the fitting results. As we're more interested in the differences induced by the perturbations than in the absolute CD numbers, only CD differences between the nominal condition and one perturbed condition are plotted. The CD values in the plot are expressed as percentages relative to the nominal feature size of N65 node, and the error bars in the plot mark the measurement uncertainties in the wafer differences, computed as the measurement uncertainties under the two different exposure conditions summed up quadratically.

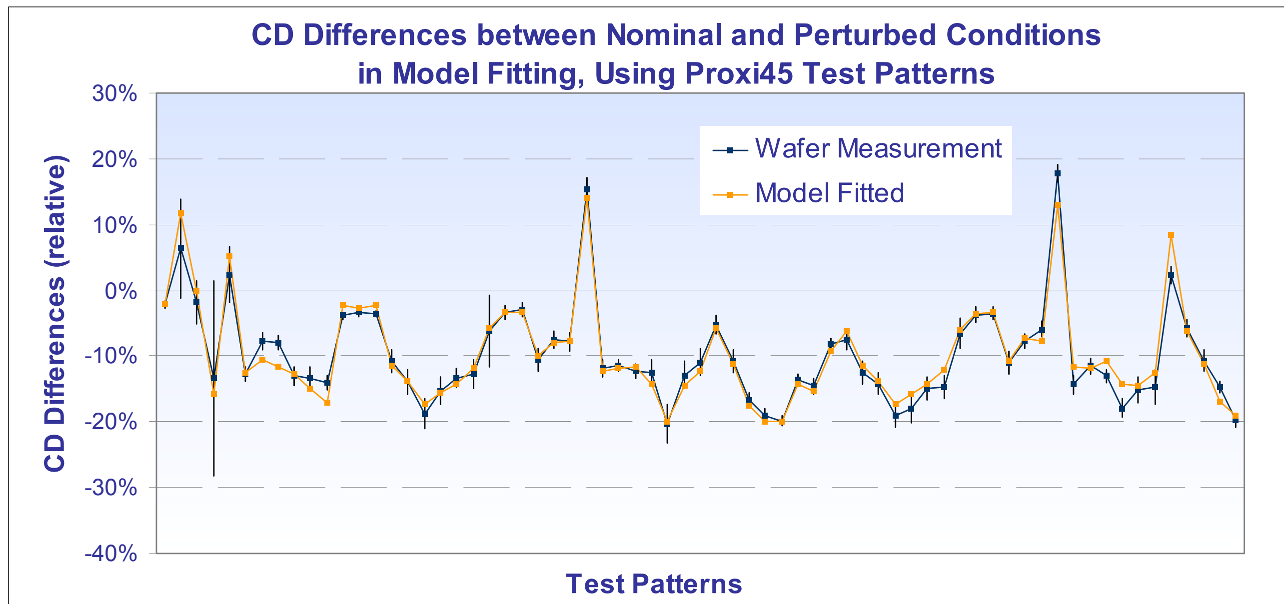

Figure 1 Wafer data versus fitted model data for CD differences between the nominal optical condition and a perturbed condition. The dark blue line marks wafer data and the yellow line, model fitting results. The CD values are expressed in percentages relative to the nominal feature size of N65 node. The error bars on the wafer data curve mark the uncertainties in the measured wafer differences.

The calibrated model is validated under a different perturbed scanner optical, using a different set of test patterns on a generic test reticle developed by tsmc for the poly layer using N65 technology. The model-predicted differences between the nominal and perturbed conditions are compared to wafer-measured results, which have not been used in the model calibration. As shown below in Figure 2, the model predictions and wafer results match well, considering the wafer measurement uncertainties.

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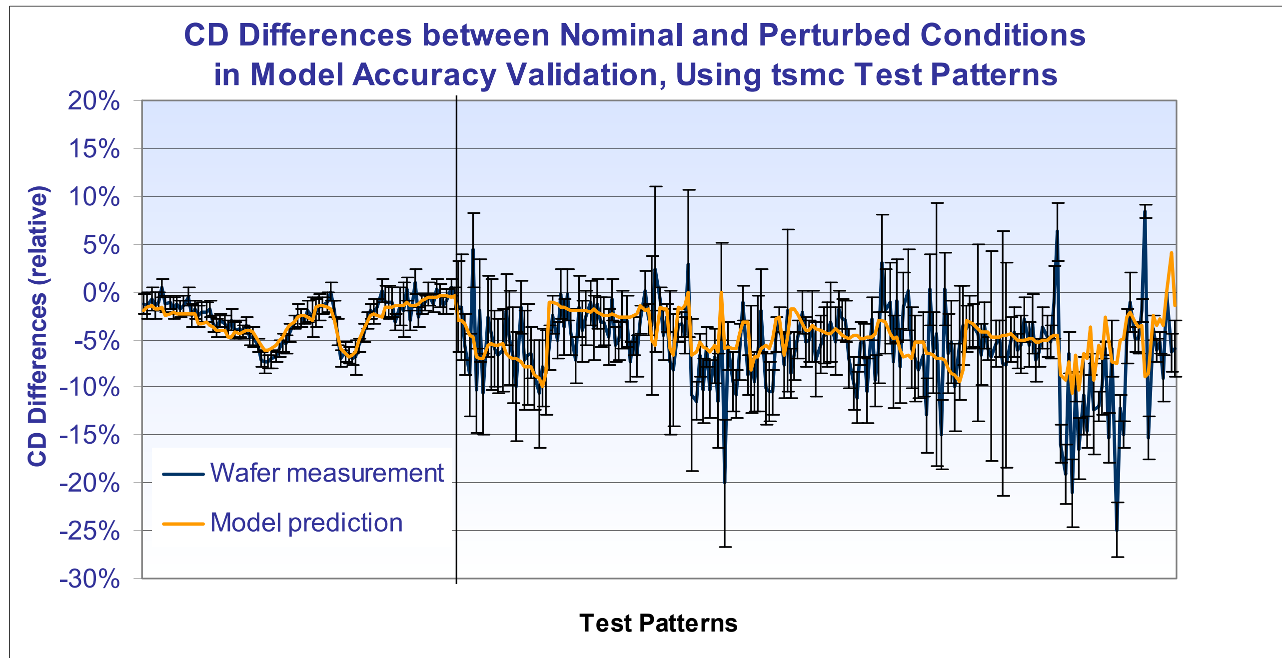

Figure 2 Wafer measurement versus model predictions for CD differences between the nominal condition and a perturbed condition. The dark blue line marks wafer data and the yellow line marks model predictions, both are relative to the nominal feature size of N65 technology node. The error bars on the wafer data indicate wafer measurement uncertainties, which are uncertainties of two independent wafer measurements summed up quadratically. The uncertainty ranges from 0.5~2nm for 1-dimensional patterns (to the left of the plot) to 1~10nm for 2-dimensional patterns (to the right of the plot).

3.3 Scanner matching

In the proof-of-concept experiments, a to-be-tuned scanner is to be matched to a reference scanner. Patterns from tsmc's test reticle are chosen as matching targets, and the goal of the scanner tuning is to minimize the difference between the two scanners in terms of imaging behavior on these patterns. A total of 283 patterns are used, among them are pre-designed generic test patterns ("1D" for 1-dimensional line/space through-pitch patterns, "2D_1", "2D_2", "2D_3", "2D_4", and "2D_5" for various 2-dimensional test patterns), patterns that have been collected from production layouts because of their vulnerability to scanner mismatches ("Category 1", "Category 2", and "Category 3"), and also 34 "matching weakness" patterns which have been identified as having the most severe mismatches between the two scanners, based on the contour-to-contour full chip simulation results, using test reticle layout GDS and the Tachyon models for the two scanners.

The matching target patterns' CD sensitivities to scanner knobs are simulated from the Tachyon model for the to-be-tuned scanner, as shown in Figure 3. The sensitivities to the different knobs have different units, so they are normalized to be dimensionless in order to be displayed in the same plot. Based on the LithoTuner methodology previously described in section 2, a set of scanner knob offsets is generated so as to minimize the overall root-mean-square (RMS) CD difference on the 283 patterns between the two scanners.

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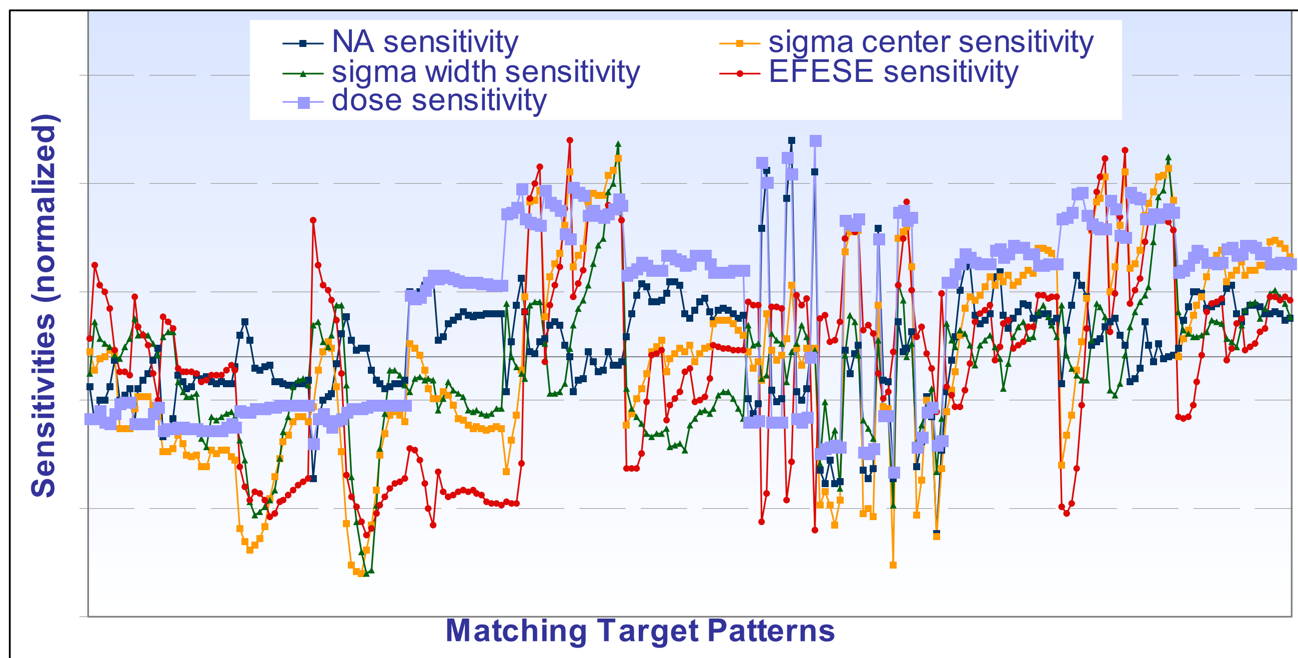

Figure 3 Matching target patterns' CD sensitivities to scanner tuning knobs, normalized in order to be displayed in the same plot. The sensitivities are derived based on a calibrated model for the to-be-tuned scanner. Sigma width represents the ring width of the annular illumination (outer sigma – inner sigma) and sigma center represents the ring center radius ((outer sigma + inner sigma)/2).

3.4 Experimental validation of the matching result

Wafer exposures are carried out using both the tuning recipe computed by LithoTuner, and a tsmc baseline tuning recipe, which has been optimized experimentally for 1D through-pitch patterns only. CD-SEM measurements on the matching target patterns are taken to verify the tuning, and the results in terms of RMS CD differences by category are shown in Figure 4. The RMS differences are expressed as percentages of the nominal feature size of N65 node in the figure. As can be seen from Figure 4, the matching on 1D patterns is already satisfactorily achieved by the tsmc baseline recipe, so the scanner tuning goal of this project is to show 2D matching improvements without degrading 1D matching. The LithoTuner recipe has indeed resulted in significant 2D matching improvements (more than 20% relative for "Category 2", "Category 3", Weakness, "2D_4" and "2D_5" categories, c.f. Figure 4) over the tsmc baseline recipe, while keeping 1D matching at the original satisfactory level. The result clearly demonstrates the capability of LithoTuner as an effective tool for reducing existing scanner performance mismatches by simulation methods employing predictive Tachyon models, while not creating new mismatch issues. In particular, the mismatching reduction on the "Weakness" patterns accentuates the LithoTuner capability of identifying patterns that are more susceptible to scanner mismatches, and proactively performing scanner tuning with these patterns taken into consideration.

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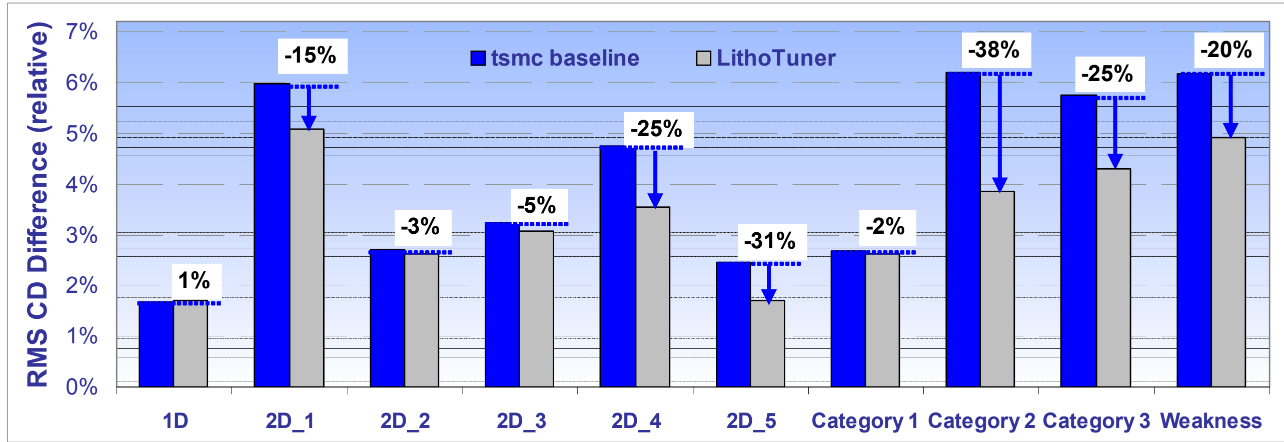

Figure 4 LithoTuner proof-of-concept results of scanner matching, in terms of wafer-measured RMS CD differences between the tuned scanner and the reference scanner. The percentage numbers above the bars mark the per-category relative RMS change between using the tsmc baseline recipe and using the LithoTuner recipe. Compared to the tsmc baseline tuning recipe, the LithoTuner results have achieved significant improvements on 2D patterns, while keeping 1D patterns closely matched.

In addition to statistics based on CD-SEM data, wafer-acceptance-test ("WAT") results and yield analysis results for a production layout are also collected using the reference scanner, the to-be-tuned scanner with the tsmc baseline tuning recipe, and the to-be-tuned scanner with the LithoTuner recipe. The WAT tests include tests on saturation current I_{sat} and threshold voltage $V_{tl,}$ and the parameter values from the reference scanner wafers are used as baselines. In Figure 5 are shown the relatively differences of the WAT parameters from the reference scanner baselines, and it is clear that the LithoTuner recipe produces closer matches to the reference scanner, especially for the saturation current. The yield analysis is performed with 3 wafers per exposure condition, and 737 dice per wafer. The yield offsets with respect to the reference scanner are shown in Figure 6, indicating that the tsmc baseline recipe leads to a ~0.55% lower yield than the reference scanner, whereas the LithoTuner recipe yield is ~0.3% higher than the reference scanner. Statistical analysis indicates that considering the size of the yield analysis datasets, the confidence level is 72% that a statistically significant gap exists in production yield between the reference scanner and the to-be-tuned scanner with tsmc baseline recipe, and the gap has been bridged by the LithoTuner tuning recipe.

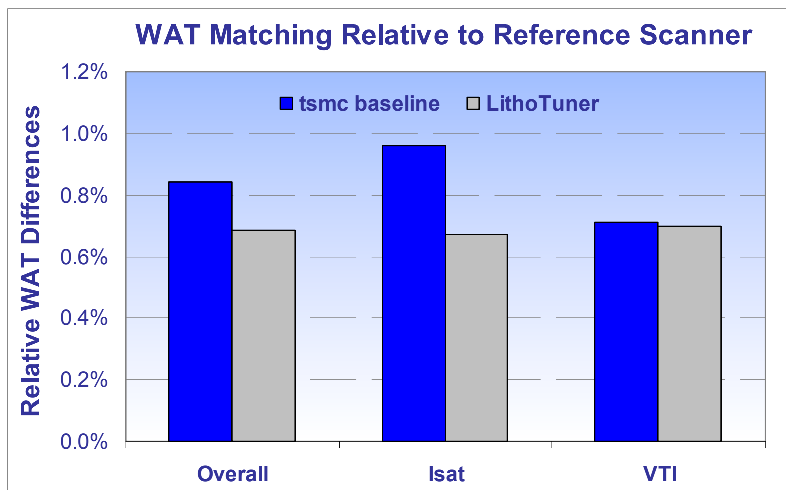

Figure 5 Wafer acceptance test results for the to-be-tuned scanner with the tsmc baseline tuning recipe and the LithoTuner tuning recipe, as compared to the WAT parameter values from the reference scanner wafers.

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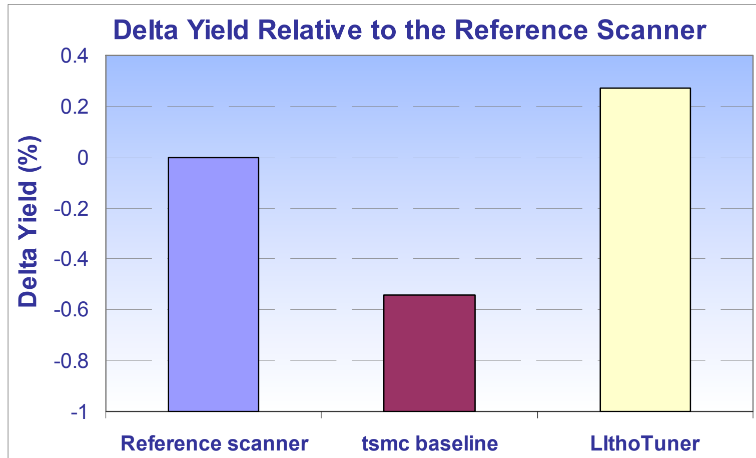

Figure 6 Yield analysis results for a N65 production layout, using the reference scanner, the to-be-tuned scanner with the tsmc baseline tuning recipe, and the to-be-tuned scanner with the LithoTuner tuning recipe. The to-be-tuned scanner yields are expressed as offsets relative to the reference scanner yield.

4. CONCLUSION

In this work, the basic concept of the LithoTuner methodology for scanner tuning is illustrated. A successful proof-of-concept scanner matching experiment is reported, in which RMS CD differences on test patterns, wafer-acceptance-test results, and yield data all confirm improvements in matching. The LithoTuner methodology is a first step toward realizing a comprehensive computational lithography regime, and can already resolve many practical lithography issues encountered daily in the fab.

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